IN THE CLAIMS:

Please note that all of the claims that remain pending and under consideration in the above-referenced application are reproduced below. This listing of claims will replace all prior versions and listings of claims in the above-referenced application.

Listing of Claims:

1. (twice amended) A semiconductor device for use in a stacked multi-chip assembly, comprising:

a semiconductor die; and

a dielectric spacer layer [comprising dielectric material], formed on at least a portion of a surface of said semiconductor die, and protruding therefrom substantially a predetermined distance that said semiconductor die and an adjacent semiconductor die of said stacked multi-chip assembly are to be spaced apart from one another, said dielectric spacer layer including voids communicating with a lateral periphery thereof.

2. (amended) The semiconductor device of claim 1, wherein said dielectric spacer layer comprises a plurality of laterally discrete spacers.

3. (original) The semiconductor device of claim 1, further comprising:

at least one discrete conductive element protruding above a surface of said semiconductor die.

4. (original) The semiconductor device of claim 3, wherein said at least one discrete conductive element comprises one of a bond wire, a thermocompression bonded lead, and a tape-automated bond element.

5. (original) The semiconductor device of claim 1, wherein said predetermined distance exceeds a distance a discrete conductive element protrudes above a surface of at least one of said semiconductor die and said adjacent semiconductor die.

6. (original) The semiconductor device of claim 1, wherein said predetermined distance is about the same as or less than a distance a discrete conductive element protrudes above a surface of at least one of said semiconductor die and said adjacent semiconductor die.

7. (amended) The semiconductor device of claim 1, wherein said dielectric spacer layer covers only a portion of said surface.

8. (amended) The semiconductor device of claim 7, wherein said dielectric spacer layer comprises a pattern.

9. (amended) The semiconductor device of claim 7, wherein said dielectric spacer layer comprises randomly arranged features.

10. (amended) The semiconductor device of claim 1, wherein said dielectric spacer layer comprises a material that will adhere to a surface of said adjacent semiconductor die.

11. (amended) The semiconductor device of claim 1, wherein said dielectric spacer layer comprises a polymer.

12. (original) The semiconductor device of claim 11, wherein said polymer comprises a photoimageable polymer.

13. (amended) The semiconductor device of claim 1, wherein said dielectric spacer layer comprises at least one of a glass, a silicon dioxide, a silicon nitride, and a silicon oxynitride.

14. (withdrawn/amended) The semiconductor device of claim 1, wherein said dielectric spacer layer is positioned on an active surface of said semiconductor die.

15. (withdrawn/amended) The semiconductor device of claim 1, wherein said dielectric spacer layer is positioned on a back side of said semiconductor die.

16. (withdrawn/amended) The semiconductor device of claim 1, further comprising: another dielectric spacer layer covering at least a portion of an opposite surface of said semiconductor die.

17. (amended) The semiconductor device of claim 1, further comprising: adhesive material on an exposed surface of said dielectric spacer layer.

18. (amended) The semiconductor device of claim 1, wherein said dielectric spacer layer comprises a plurality of at least partially superimposed, contiguous, adhered sublayers.

19. (previously amended) A semiconductor device assembly, comprising:
a first semiconductor device;
a nonconfluent spacer layer comprising dielectric material and being positioned on a surface of said first semiconductor device; and
a second semiconductor device positioned over said first semiconductor device, a surface of said second semiconductor device being adhered to said nonconfluent spacer layer.

20. (original) The semiconductor device assembly of claim 19, wherein said nonconfluent spacer layer comprises at least one void therein that communicates with a lateral periphery of said nonconfluent spacer layer.

21. (original) The semiconductor device assembly of claim 20, wherein said at least one void facilitates lateral introduction of adhesive material between said first and second semiconductor devices.

22. (original) The semiconductor device assembly of claim 19, wherein said nonconfluent spacer layer comprises a plurality of laterally discrete spacers.

23. (original) The semiconductor device assembly of claim 19, wherein said nonconfluent spacer layer has a substantially uniform thickness.

24. (original) The semiconductor device assembly of claim 19, further comprising:

at least one discrete conductive element protruding above a surface of at least one of said first and second semiconductor devices and located at least partially between said first and second semiconductor devices.

25. (original) The semiconductor device assembly of claim 24, wherein said nonconfluent spacer layer has a thickness that spaces said first and second semiconductor devices apart from one another a distance that exceeds a height said at least one discrete conductive element protrudes above said surface of at least one of said first and second semiconductor devices.

26. (original) The semiconductor device assembly of claim 24, wherein said nonconfluent spacer layer has a thickness that spaces said first and second semiconductor devices apart from one another a distance that is about the same as or less than a height said at least one discrete conductive element protrudes above said surface of at least one of said first and second semiconductor devices.

27. (withdrawn) The semiconductor device assembly of claim 19, wherein said nonconfluent spacer layer comprises dielectric material.

28. (withdrawn) The semiconductor device assembly of claim 19, wherein said nonconfluent spacer layer comprises a polymer.

29. (withdrawn) The semiconductor device assembly of claim 28, wherein said polymer adheres to surfaces of said first semiconductor device and said second semiconductor device.

30. (withdrawn) The semiconductor device assembly of claim 28, wherein said polymer comprises a photoimageable polymer.

31. (original) The semiconductor device assembly of claim 19, wherein said nonconfluent spacer layer comprises a plurality of at least partially superimposed, contiguous, mutually adhered sublayers.

32. (original) The semiconductor device assembly of claim 19, wherein said nonconfluent spacer layer comprises at least one of a glass, a silicon oxide, a silicon nitride, and a silicon oxynitride.

33. (original) The semiconductor device assembly of claim 19, wherein said nonconfluent spacer layer comprises a pattern.

34. (withdrawn) The semiconductor device assembly of claim 19, wherein said nonconfluent spacer layer comprises randomly arranged features.

35. (withdrawn) The semiconductor device assembly of claim 19, further comprising: an adhesive material securing said nonconfluent spacer layer to at least one of said surface of said first semiconductor device and said surface of said second semiconductor device.

36. (withdrawn) The semiconductor device assembly of claim 35, wherein said adhesive material is located within voids in said nonconfluent spacer layer.

37. (original) The semiconductor device assembly of claim 19, further comprising: a substrate upon which one of said first semiconductor device and said second semiconductor device is positioned.

38. (original) The semiconductor device assembly of claim 37, wherein at least one bond pad of at least one of said first semiconductor device and said second semiconductor device is in communication with a corresponding contact area of said substrate.

39. (original) The semiconductor device assembly of claim 37, wherein said substrate comprises at least one of a circuit board, an interposer, another semiconductor device, and leads.

40. (original) The semiconductor device assembly of claim 19, wherein said nonconfluent spacer layer is positioned between an active surface of said first semiconductor device and a back side of said second semiconductor device.

41. (withdrawn) The semiconductor device assembly of claim 19, further comprising: at least one additional semiconductor device.

42. (original) The semiconductor device assembly of claim 19, further comprising: a plurality of nonconfluent spacer layers between said first and second semiconductor devices, additive thicknesses of said plurality of nonconfluent spacer layers defining a distance said first and second semiconductor devices are spaced apart from one another.

43. (original) The semiconductor device assembly of claim 42, wherein a first nonconfluent spacer layer of said plurality of nonconfluent spacer layers is secured to a surface of said first semiconductor device and a second nonconfluent spacer layer of said plurality of nonconfluent spacer layers is secured to an opposed surface of said second semiconductor device.

44. (original) The semiconductor device assembly of claim 42, wherein at least some solid regions of each of said plurality of nonconfluent spacer layers are at least partially superimposed relative to one another.

45. (withdrawn) A multi-chip module, comprising:
a substrate;
a first semiconductor device positioned on said substrate;
a nonconfluent layer comprising dielectric material over said first semiconductor device;
a second semiconductor device positioned over said nonconfluent layer; and
an encapsulant covering at least portions of said first semiconductor device, said nonconfluent layer, said second semiconductor device, and portions of said substrate located adjacent said first semiconductor device.

46. (withdrawn) The multi-chip module of claim 45, wherein said substrate comprises at least one of a circuit board, an interposer, another semiconductor device, and leads.

47. (withdrawn) The multi-chip module of claim 45, wherein at least one bond pad of at least one of said first semiconductor device and said second semiconductor device is in electrical communication with a corresponding contact area of said substrate.

48. (withdrawn) The multi-chip module of claim 47, wherein said electrical communication is established by at least one discrete conductive element extending at least partially between said first and second semiconductor devices and protruding above a surface of at least one of said first semiconductor device and said second semiconductor device.

49. (withdrawn) The multi-chip module of claim 48, wherein said nonconfluent layer has a thickness that exceeds a distance said at least one discrete conductive element protrudes above said surface.

50. (withdrawn) The multi-chip module of claim 48, wherein a thickness of said nonconfluent layer is about the same as or less than a distance said at least one discrete conductive element protrudes above said surface.

51. (withdrawn) The multi-chip module of claim 45, wherein said nonconfluent spacer layer comprises a plurality of laterally discrete spacers.

52. (withdrawn) The multi-chip module of claim 45, wherein said nonconfluent layer comprises a pattern.

53. (withdrawn) The multi-chip module of claim 45, wherein said nonconfluent layer comprises randomly arranged features.

54. (withdrawn) The multi-chip module of claim 45, wherein said nonconfluent layer has a substantially consistent height.

55. (withdrawn) The multi-chip module of claim 45, wherein said nonconfluent layer comprises a dielectric material.

56. (withdrawn) The multi-chip module of claim 55, wherein said dielectric material comprises at least one of a glass, a silicon oxide, a silicon nitride, and a silicon oxynitride.

57. (withdrawn) The multi-chip module of claim 45, wherein said nonconfluent layer comprises a polymer.

58. (withdrawn) The multi-chip module of claim 57, wherein said polymer is capable of adhering to a surface of at least one of said first semiconductor device and said second semiconductor device.

59. (withdrawn) The multi-chip module of claim 57, wherein said polymer comprises a photoimageable polymer.

60. (withdrawn) The multi-chip module of claim 45, wherein said nonconfluent layer comprises a plurality of at least partially superimposed, contiguous, mutually adhered layers.

61. (withdrawn) The multi-chip module of claim 45, further comprising:
an adhesive material securing said first and second semiconductor devices to one another.

62. (withdrawn) The multi-chip module of claim 61, wherein said adhesive material is located within voids of said nonconfluent layer.

63. (withdrawn) The multi-chip module of claim 45, wherein said encapsulant comprises a glob-top type encapsulant.

64. (withdrawn) The multi-chip module of claim 45, wherein said encapsulant comprises a molded encapsulant.

65. (withdrawn) The multi-chip module of claim 45, further comprising:
a plurality of nonconfluent layers between said first and second semiconductor devices, additive thicknesses of said plurality of nonconfluent layers defining a distance said first and second semiconductor devices are spaced apart from one another.

66. (withdrawn) The multi-chip module of claim 65, wherein a first nonconfluent layer of said plurality of nonconfluent layers is secured to a surface of said first semiconductor device and a second nonconfluent layer of said plurality of nonconfluent layers is secured to an opposed surface of said second semiconductor device.

67. (withdrawn) The multi-chip module of claim 65, wherein at least some solid regions of each of said plurality of nonconfluent layers are at least partially superimposed relative to one another.

68-102. (cancelled)